

FIGURE 1A
(PRIOR ART)

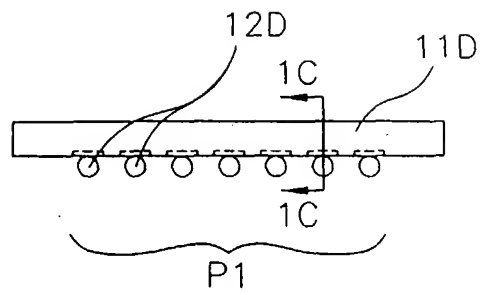


FIGURE 1B
(PRIOR ART)

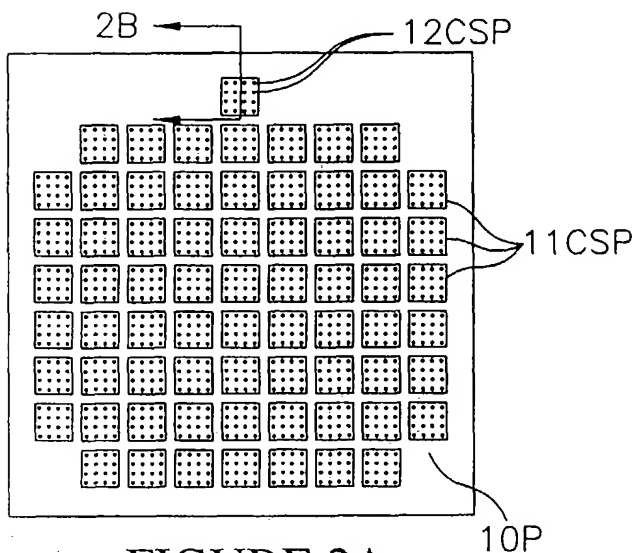


FIGURE 2A
(PRIOR ART)

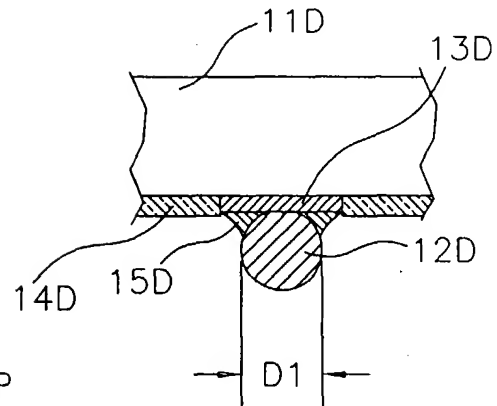


FIGURE 1C
(PRIOR ART)

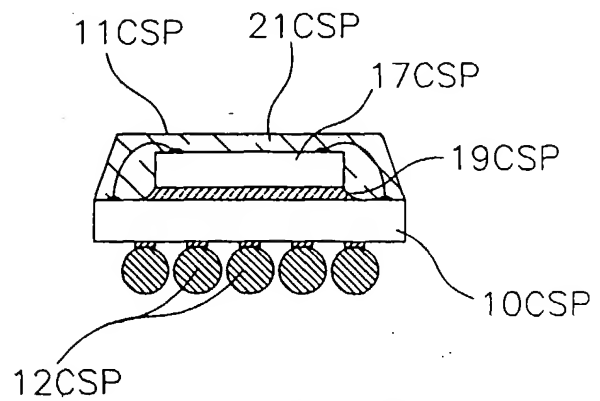


FIGURE 2B
(PRIOR ART)

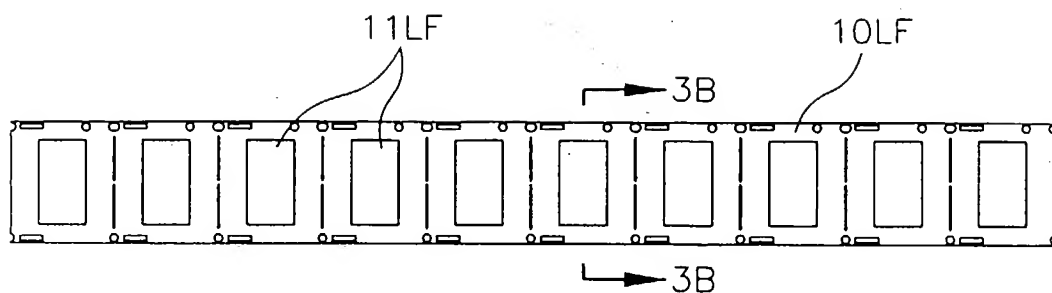


FIGURE 3A
(PRIOR ART)

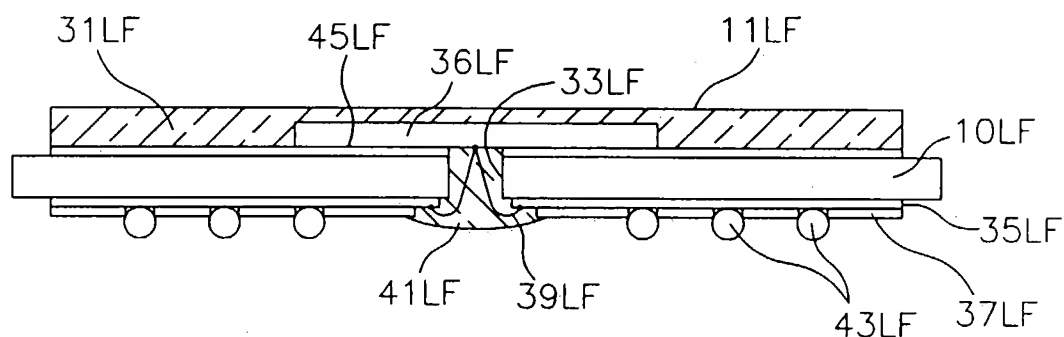


FIGURE 3B
(PRIOR ART)

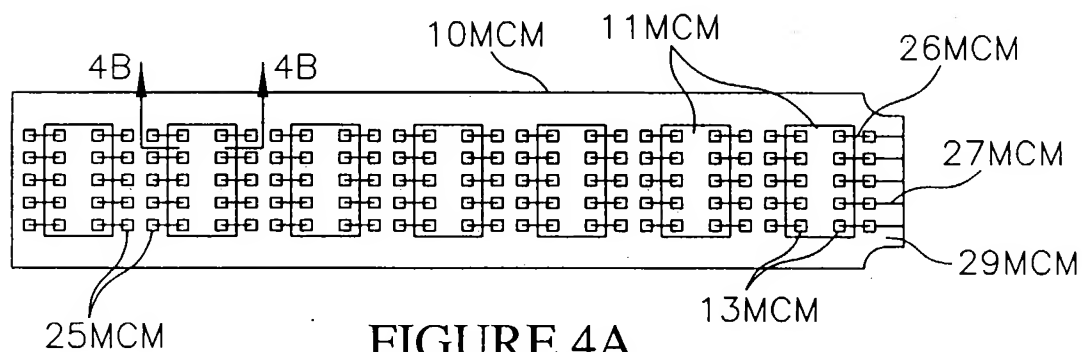


FIGURE 4A
(PRIOR ART)

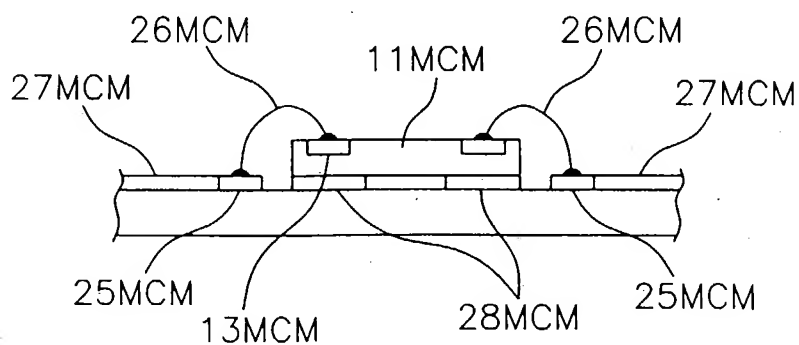
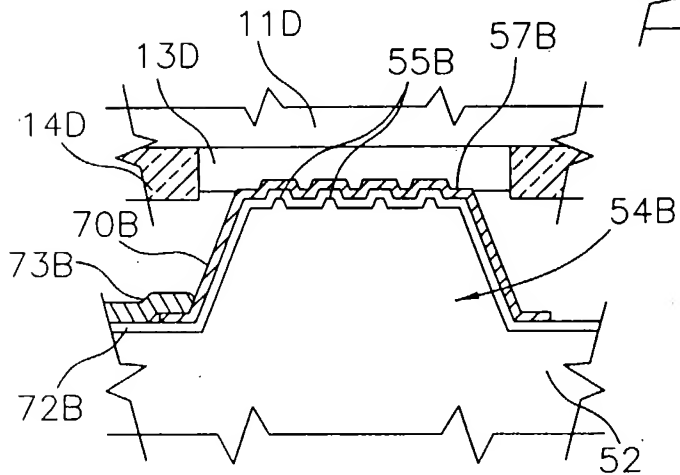
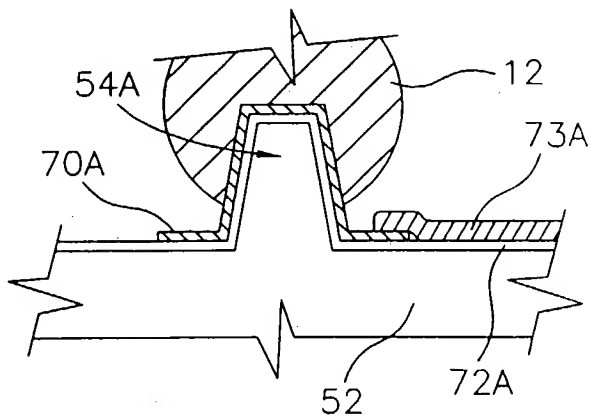
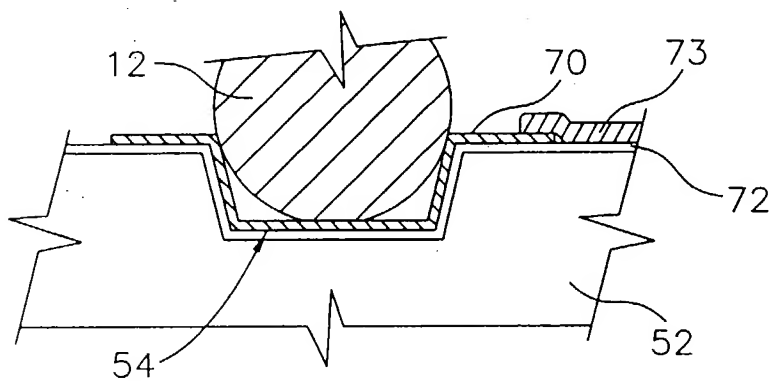
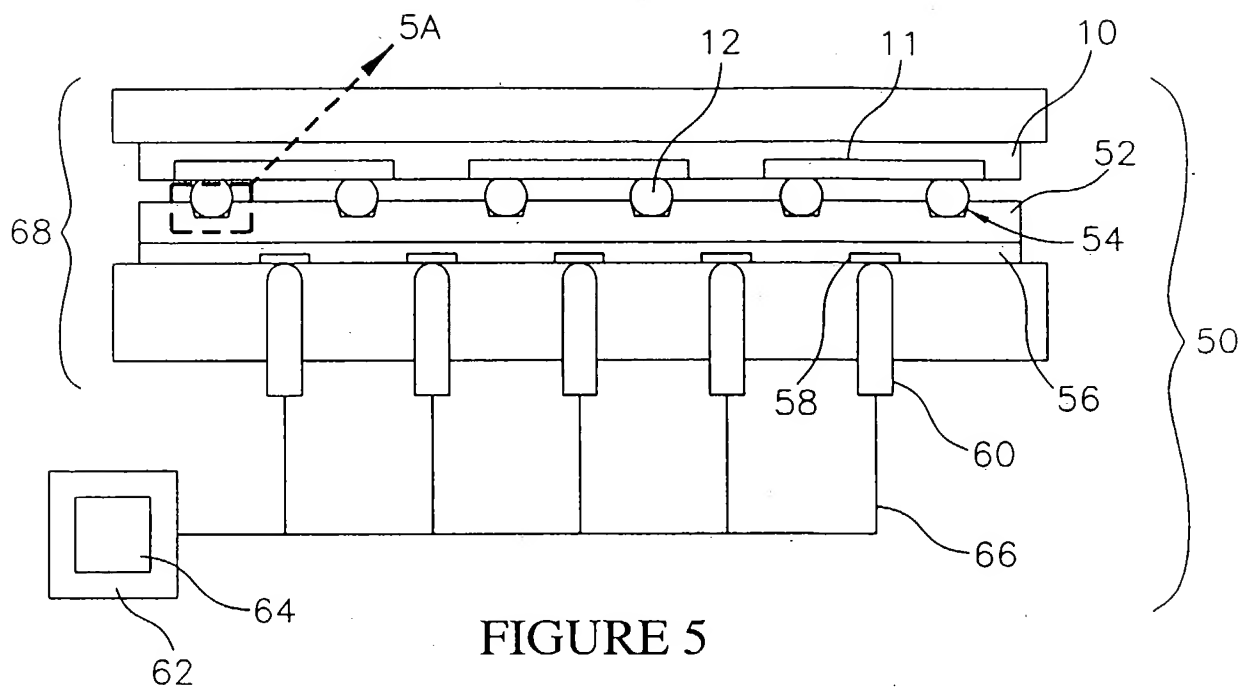


FIGURE 4B
(PRIOR ART)



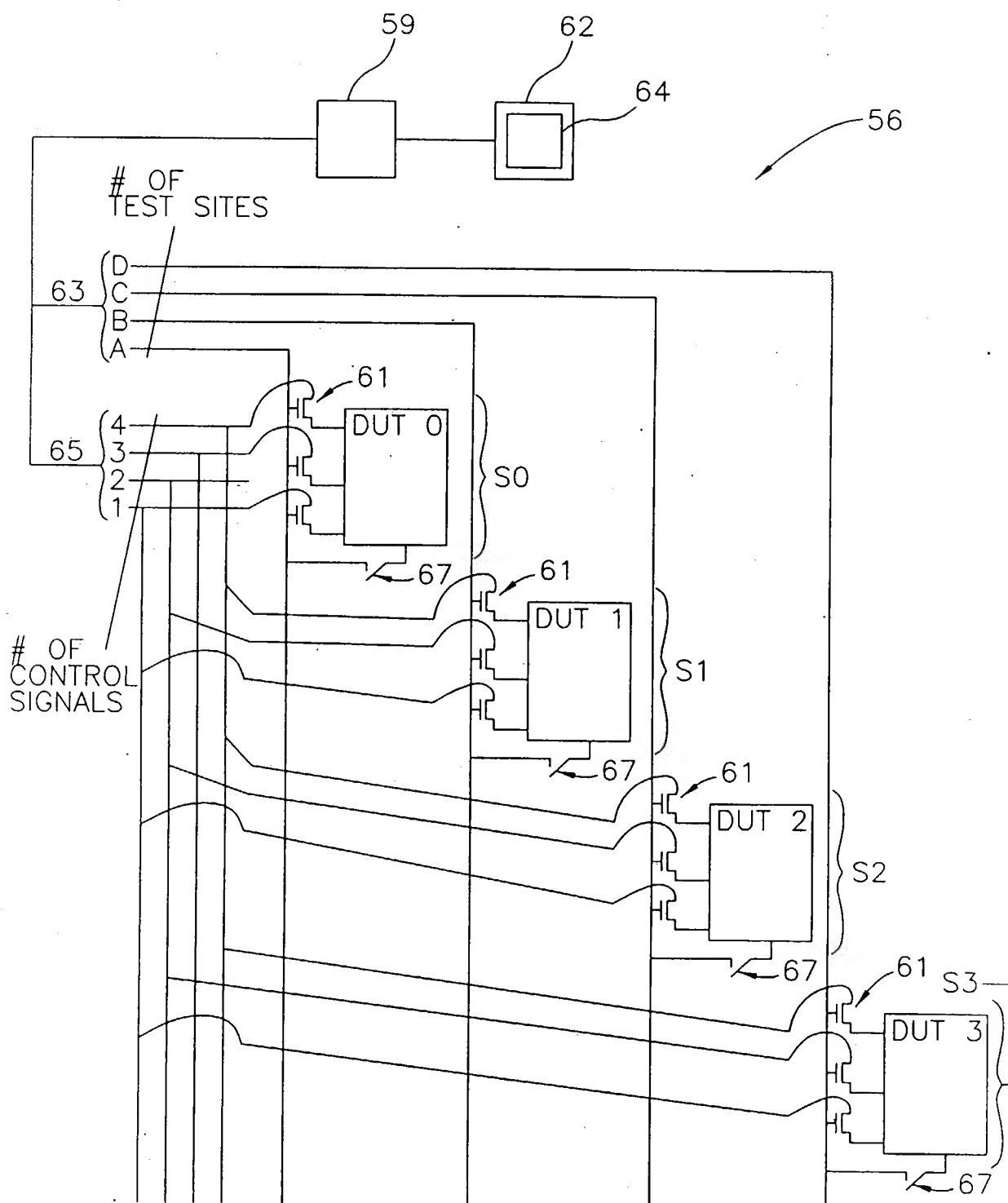


FIGURE 6

ALIGN THE COMPONENT CONTACTS 12 TO THE INTERCONNECT CONTACTS 54.

PLACE THE COMPONENT CONTACTS 12 AND THE INTERCONNECT CONTACTS 54 IN PHYSICAL AND ELECTRICAL CONTACT.

TRANSMIT TEST SIGNALS FOR PERFORMING FUNCTIONALITY TESTS (e.g., OPENS AND SHORTS) THROUGH THE INTERCONNECT CONTACTS 54 TO SELECTED COMPONENTS 11 USING THE SWITCHED NETWORK 56 TO MULTIPLY AND SELECTIVELY TRANSMIT THE TEST SIGNALS.

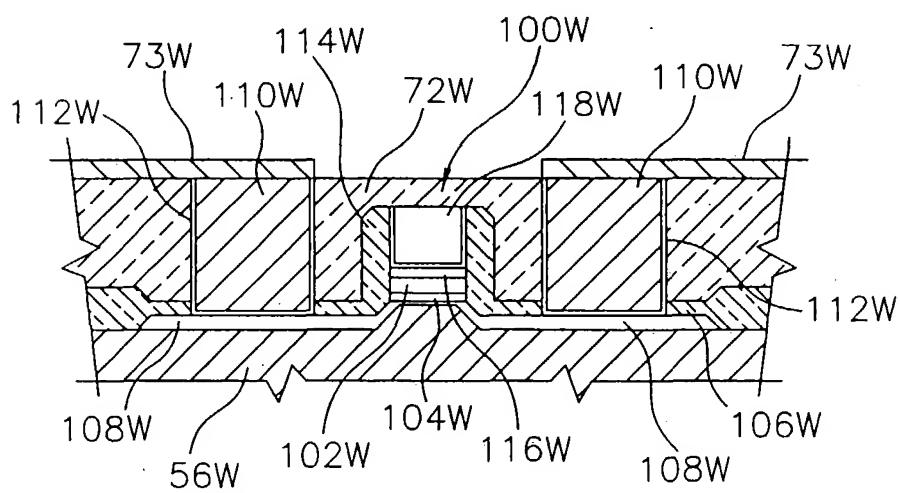
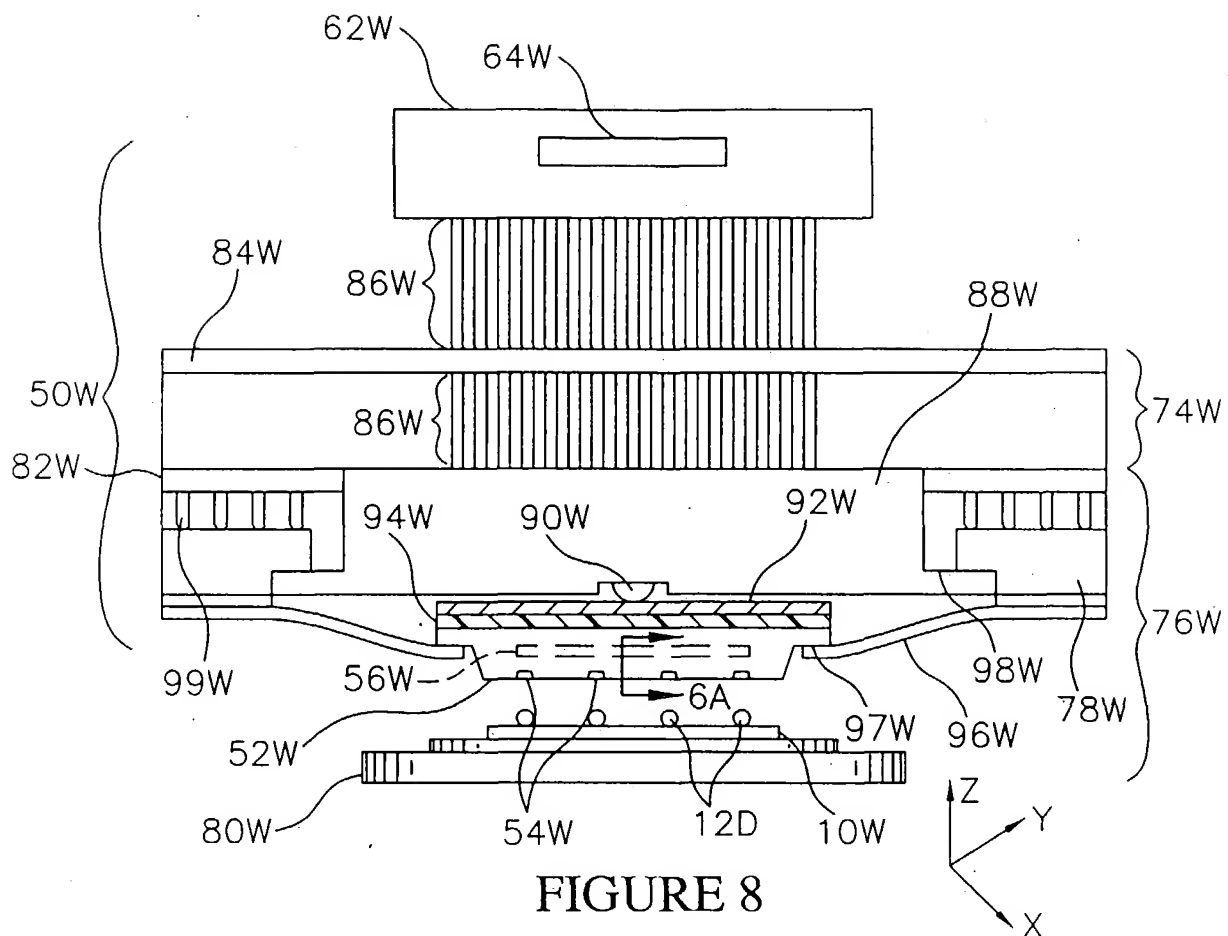
ELECTRICALLY ISOLATE ANY DEFECTIVE OR NONFUNCTIONAL COMPONENTS 11 USING THE SWITCHED NETWORK 56.

TRANSMIT "WRITE" TEST SIGNALS FOR PERFORMING PARAMETRIC TESTING (e.g., SPEED GRADING) THROUGH THE INTERCONNECT CONTACTS 54 TO SELECTED COMPONENTS 11 USING THE SWITCHED NETWORK 56 TO MULTIPLY AND SELECTIVELY TRANSMIT THE WRITE TEST SIGNALS.

TRANSMIT "READ" TEST SIGNALS FROM SELECTED GROUPS OF COMPONENTS 11 UP TO THE LIMIT OF TESTER RESOURCES USING THE SWITCHED NETWORK 56 TO GROUP THE COMPONENTS 11 AS REQUIRED.

OPTIONALLY, TRANSMIT BURN-IN TEST SIGNALS TO THE COMPONENTS 11 USING THE SWITCHED NETWORK 56 TO ELECTRICALLY ISOLATE DEFECTIVE COMPONENTS 11.

FIGURE 7



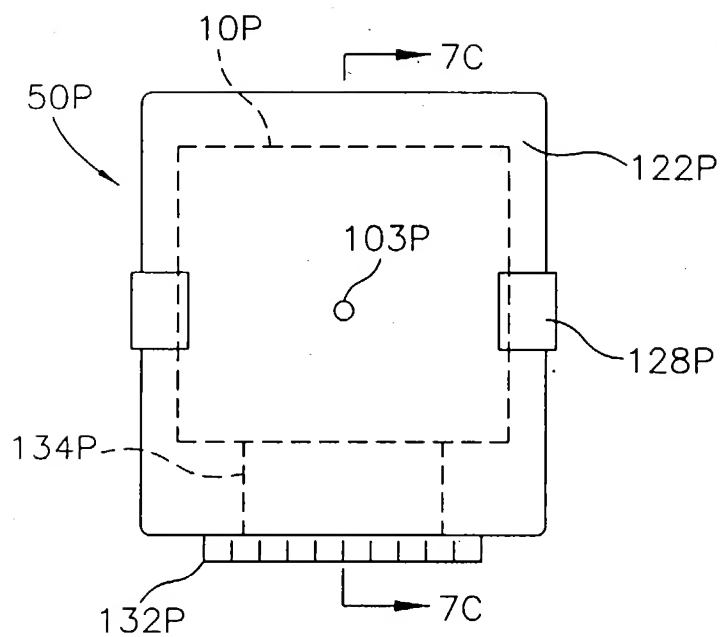


FIGURE 9A

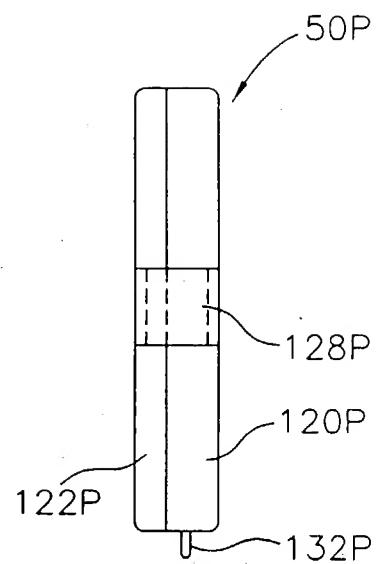


FIGURE 9B

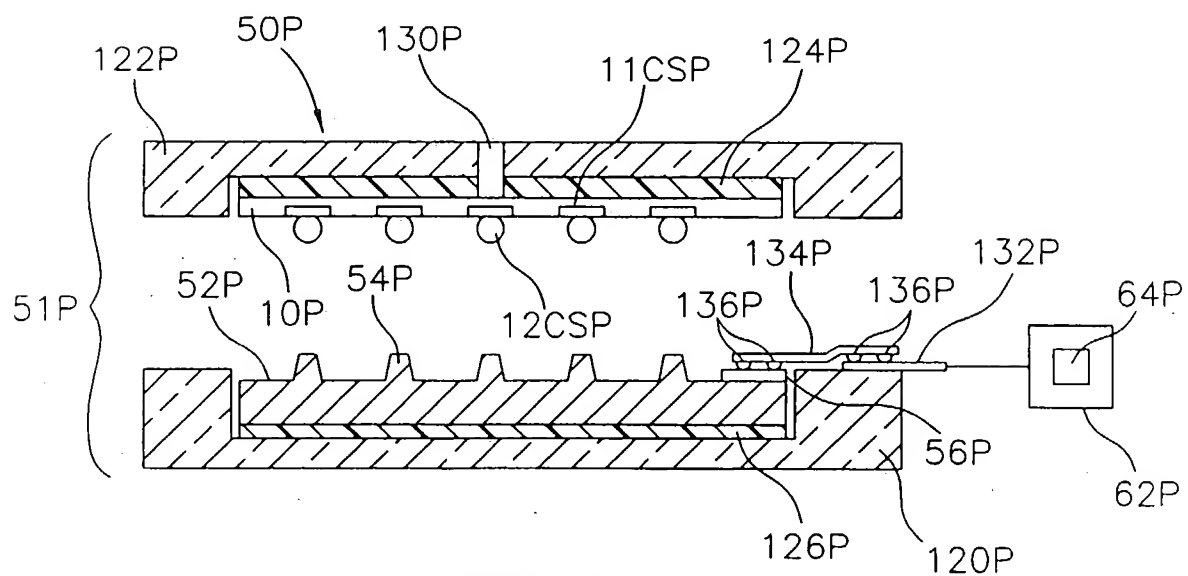


FIGURE 9C

